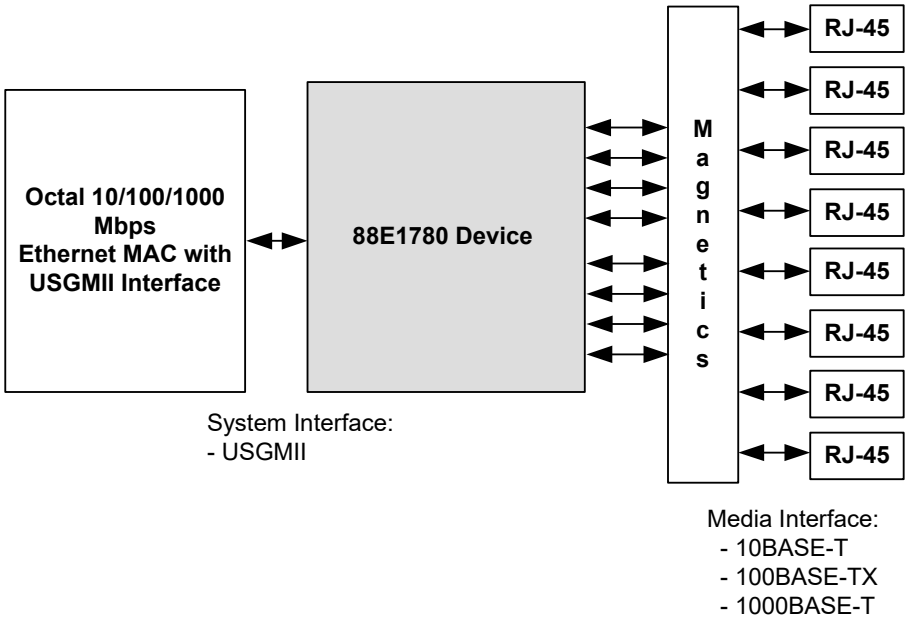
Marvell® Alaska® 88E1780

Integrated Octal 10/100/1000 Mbps Energy Efficient Ethernet Transceiver

Datasheet - Public

Doc. No. TD-000923 Rev. 1
October 5, 2020
Document Classification: Public

Figure 1: 88E1780 Device Application - USGMII (System) to Copper



1 Signal Description

1.1 Pin Description

Table 1: Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

1.1.1 88E1780 128-Pin LQFP Package Pinout

Figure 2: 88E1780 Device 128-Pin LQFP Package with EPAD (Top View)

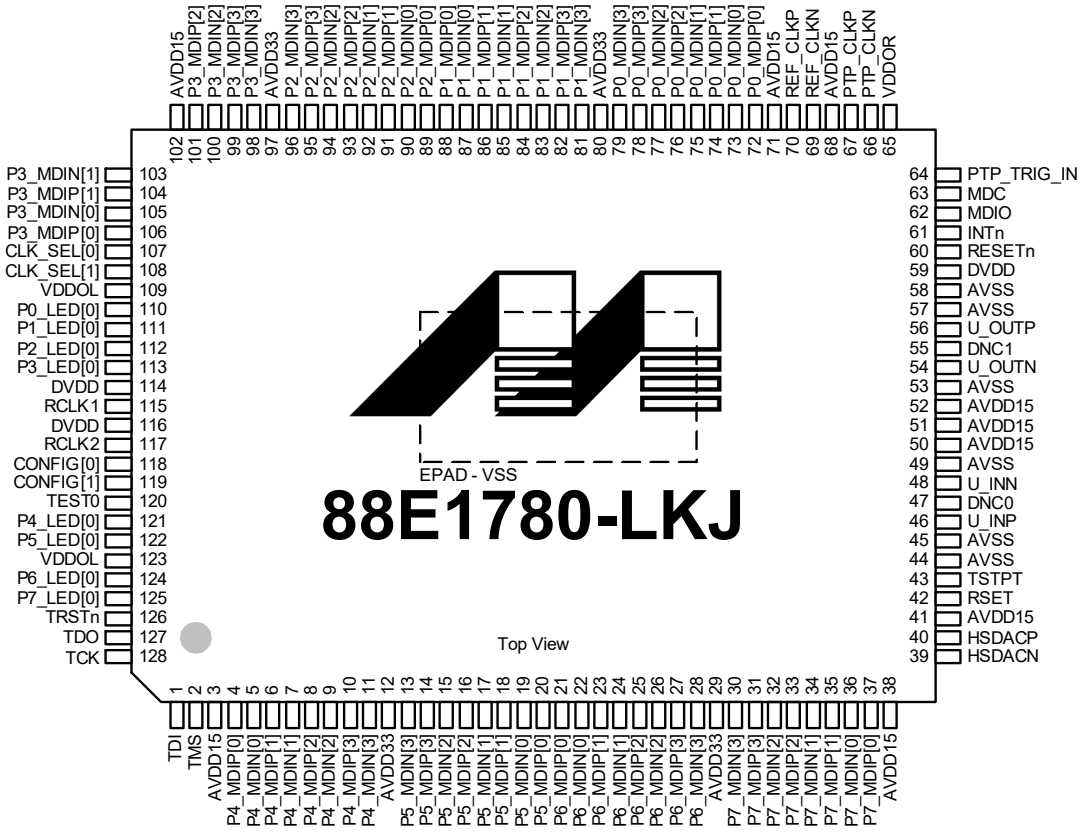


Table 2: Media Dependent Interface Port 0

88E1780 Pin #	Pin Name	Pin Type	Description
72 73	P0_MDIP[0] P0_MDIN[0]	I/O	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] correspond to BI_DA±. In MDIX configuration, MDIP/N[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[0] pins.
74 75	P0_MDIP[1] P0_MDIN[1]	I/O	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] correspond to BI_DB±. In MDIX configuration, MDIP/N[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[1] pins.
76 77	P0_MDIP[2] P0_MDIN[2]	I/O	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] correspond to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[2] pins.
78 79	P0_MDIP[3] P0_MDIN[3]	I/O	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] correspond to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. **NOTE:** Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[3] pins.

Table 3: Media Dependent Interface Port 1

88E1780 Pin #	Pin Name	Pin Type	Description
88 87	P1_MDIP[0] P1_MDIN[0]	I/O	Media Dependent Interface[0] for Port 1. Refer to P0_MDI[0]P/N.
86 85	P1_MDIP[1] P1_MDIN[1]	I/O	Media Dependent Interface[1] for Port 1. Refer to P0_MDI[1]P/N.
84 83	P1_MDIP[2] P1_MDIN[2]	I/O	Media Dependent Interface[2] for Port 1. Refer to P0_MDI[2]P/N.
82 81	P1_MDIP[3] P1_MDIN[3]	I/O	Media Dependent Interface[3] for Port 1. Refer to P0_MDI[3]P/N.

Table 4: Media Dependent Interface Port 2

88E1780 Pin #	Pin Name	Pin Type	Description
89 90	P2_MDIP[0] P2_MDIN[0]	I/O	Media Dependent Interface[0] for Port 2. Refer to P0_MDI[0]P/N.
91 92	P2_MDIP[1] P2_MDIN[1]	I/O	Media Dependent Interface[1] for Port 2. Refer to P0_MDI[1]P/N.
93 94	P2_MDIP[2] P2_MDIN[2]	I/O	Media Dependent Interface[2] for Port 2. Refer to P0_MDI[2]P/N.
95 96	P2_MDIP[3] P2_MDIN[3]	I/O	Media Dependent Interface[3] for Port 2. Refer to P0_MDI[3]P/N.

Table 5: Media Dependent Interface Port 3

88E1780 Pin #	Pin Name	Pin Type	Description
106 105	P3_MDIP[0] P3_MDIN[0]	I/O	Media Dependent Interface[0] for Port 3. Refer to P0_MDI[0]P/N.
104 103	P3_MDIP[1] P3_MDIN[1]	I/O	Media Dependent Interface[1] for Port 3. Refer to P0_MDI[1]P/N.
101 100	P3_MDIP[2] P3_MDIN[2]	I/O	Media Dependent Interface[2] for Port 3. Refer to P0_MDI[2]P/N.
99 98	P3_MDIP[3] P3_MDIN[3]	I/O	Media Dependent Interface[3] for Port 3. Refer to P0_MDI[3]P/N.

Table 6: Media Dependent Interface Port 4

88E1780 Pin #	Pin Name	Pin Type	Description
4 5	P4_MDIP[0] P4_MDIN[0]	I/O	Media Dependent Interface[0] for Port 4. Refer to P0_MDI[0]P/N.
6 7	P4_MDIP[1] P4_MDIN[1]	I/O	Media Dependent Interface[1] for Port 4. Refer to P0_MDI[1]P/N.
8 9	P4_MDIP[2] P4_MDIN[2]	I/O	Media Dependent Interface[2] for Port 4. Refer to P0_MDI[2]P/N.
10 11	P4_MDIP[3] P4_MDIN[3]	I/O	Media Dependent Interface[3] for Port 4. Refer to P0_MDI[3]P/N.

Table 7: Media Dependent Interface Port 5

88E1780 Pin #	Pin Name	Pin Type	Description
20 19	P5_MDIP[0] P5_MDIN[0]	I/O	Media Dependent Interface[0] for Port 5. Refer to P0_MDI[0]P/N.
18 17	P5_MDIP[1] P5_MDIN[1]	I/O	Media Dependent Interface[1] for Port 5. Refer to P0_MDI[1]P/N.
16 15	P5_MDIP[2] P5_MDIN[2]	I/O	Media Dependent Interface[2] for Port 5. Refer to P0_MDI[2]P/N.
14 13	P5_MDIP[3] P5_MDIN[3]	I/O	Media Dependent Interface[3] for Port 5. Refer to P0_MDI[3]P/N.

Table 8: Media Dependent Interface Port 6

88E1780 Pin #	Pin Name	Pin Type	Description
21 22	P6_MDIP[0] P6_MDIN[0]	I/O	Media Dependent Interface[0] for Port 6. Refer to P0_MDI[0]P/N.
23 24	P6_MDIP[1] P6_MDIN[1]	I/O	Media Dependent Interface[1] for Port 6. Refer to P0_MDI[1]P/N.
25 26	P6_MDIP[2] P6_MDIN[2]	I/O	Media Dependent Interface[2] for Port 6. Refer to P0_MDI[2]P/N.
27 28	P6_MDIP[3] P6_MDIN[3]	I/O	Media Dependent Interface[3] for Port 6. Refer to P0_MDI[3]P/N.

Table 9: Media Dependent Interface Port 7

88E1780 Pin #	Pin Name	Pin Type	Description
37 36	P7_MDIP[0] P7_MDIN[0]	I/O	Media Dependent Interface[0] for Port 7. Refer to P0_MDI[0]P/N.
35 34	P7_MDIP[1] P7_MDIN[1]	I/O	Media Dependent Interface[1] for Port 7. Refer to P0_MDI[1]P/N.
33 32	P7_MDIP[2] P7_MDIN[2]	I/O	Media Dependent Interface[2] for Port 7. Refer to P0_MDI[2]P/N.
31 30	P7_MDIP[3] P7_MDIN[3]	I/O	Media Dependent Interface[3] for Port 7. Refer to P0_MDI[3]P/N.

Table 10: USGMII Interface

88E1780 Pin #	Pin Name	Pin Type	Description
46 48	U_INP U_INN	I	USGMII Transmit Data. 10 GBaud input - Positive and Negative. AC Coupling connection must be used for the USGMII interface. 0.1uF is recommended for each of the USGMII signals. DC Coupling connection is not supported for the USGMII interface.
56 54	U_OUTP U_OUTN	O	USGMII Receive Data. 10 GBaud output - Positive and Negative. AC Coupling connection must be used for the USGMII interface. 0.1uF is recommended for each of the USGMII signals. DC Coupling connection is not supported for the USGMII interface.

Table 11: Synchronous Ethernet Interface/PTP

88E1780 Pin #	Pin Name	Pin Type	Description
115	RCLK1	O	First 25/125 MHz Recovered Clock.
117	RCLK2	O	Second 25/125 MHz Recovered Clock.
64	PTP_TRIG_IN	I	PTP event request input.

Table 12: Management Interface/Control

88E1780 Pin #	Pin Name	Pin Type	Description
63	MDC	I	Management Clock pin. MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 25 MHz.
62	MDIO	I/O	Management Data pin. MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.
61	INTn	OD	Interrupt pin. INTn functions as an active low interrupt output. This pin requires a pull-up resister. The pull-up resistor used for the INTn pin should not be connected to voltage higher than VDDOR.

Table 13: LED/Configuration

88E1780 Pin #	Pin Name	Pin Type	Description
110 111 112 113 121 122 124 125	P0_LED P1_LED P2_LED P3_LED P4_LED P5_LED P6_LED P7_LED	O	Parallel LED Output Port 0 to Port 7. Matrix LED Input/Output Port 0 to Port 7.
118	CONFIG[0]	I	Global hardware configuration. See Section 2.3.1, Hardware Configuration, on page 24 for details.
119	CONFIG[1]	I	

Table 14: JTAG

88E1780 Pin #	Pin Name	Pin Type	Description
1	TDI	I, PU	Boundary scan test data input. TDI contains an internal 150 kohm pull-up resistor.
2	TMS	I, PU	Boundary scan test mode select input. TMS contains an internal 150 kohm pull-up resistor.
128	TCK	I, PU	Boundary scan test clock input. TCK contains an internal 150 kohm pull-up resistor.
126	TRSTn	I, PU	Boundary scan test reset input. Active low. TRSTn contains an internal 150 kohm pull-up resistor. For normal operation, TRSTn should be pulled low with a 4.7 kohm pull-down resistor.
127	TDO	O	Boundary scan test data output.

Table 15: Clock/Reset

88E1780 Pin #	Pin Name	Pin Type	Description
70 69	REF_CLKP REF_CLKN	I	125 MHz/156.25 MHz Reference Clock Input Positive and Negative +/- 50 ppm tolerance differential clock inputs. The inputs are LVDS differential inputs with a 100 ohm differential internal termination resistor and internal ac-coupling. REF_CLKP/N also supports 125 MHz single-ended clock. In this case, the unused pin must be connected with 0.1uF capacitor to ground. The reference clock input voltage level should not be higher than AVDD15. The following REF_CLK inputs are supported: • 156.25 MHz LVDS REF_CLKP/N • 125 MHz LVDS REF_CLKP/N
67 66	PTP_CLKP PTP_CLKN	I	PCH time stamp clock.
108 107	CLK_SEL[1] CLK_SEL[0]	I	Reference Clock Selection CLK_SEL[1:0] 00 = Use 156.25 MHz REF_CLKP/N 01 = Use 125 MHz REF_CLKP/N 10 = Reserved 11 = Reserved CLK_SEL[1:0] must be connected to VDDOL for configuration HIGH.
60	RESETn	I	Hardware reset. The reference clock must be active for a minimum of 10 clock cycles before the rising edge of RESETn. RESETn must be in inactive state for normal operation. 1 = Normal operation 0 = Reset

Table 16: Test

88E1780 Pin #	Pin Name	Pin Type	Description
40 39	HSDACP HSDACN	O	AC Test Points (Positive and Negative), TX_TCLK. The HSDACP/N outputs are used for AC Test Points and TX_TCLK. These pins must be connected to a 50 ohm termination resistor to VSS. These pins can be left floating if not used for IEEE testing, and debug test points are not of importance.
43	TSTPT	O	Pin should be left floating.
120	TEST0	I	Tie to ground with a 4.7 kohm resistor.

Table 17: Reference

88E1780 Pin #	Pin Name	Pin Type	Description
42	RSET	I	Resistor Reference External 5.0 kohm 1% resistor connected to ground.

Table 18: Power & Ground

88E1780 Pin #	Pin Name	Pin Type	Description
59 114 116	DVDD	Power	1.15V Digital Supply
3 38 41 50 51 52 68 71 102	AVDD15	Power	1.5V Analog Supply[1].
12 29 80 97	AVDD33	Power	3.3V Analog Supply.
109 123	VDDOL	Power	2.5V or 3.3V I/O Supply[2]. **NOTE:** The I/O voltage supplied by VDDOL is not tolerant to any other voltage levels.
65	VDDOR	Power	1.8V, 2.5V, or 3.3V I/O Supply[3]. The I/O supplied by the VDDOR is not tolerant to any other voltage levels.
44 45 49 53 57 58	AVSS	Ground	Ground.
EPAD	VSS	Ground	Ground to device. The device is packaged in a 128-pin LQFP package with an EPAD (exposed die pad) on the bottom of the package. This EPAD must be soldered to VSS as it is the main VSS connection on the device. The location and dimensions of the EPAD can be found in Table 53. See the Marvell® EPAD Layout Guidelines Application Note for EPAD layout details.

1. AVDD15 supplies analog core, REFCLKP, REFCLKN, TSTPT, PTP_CLKP, PTP_CLKN, RSET, HSDACP, and HSDACN.
2. VDDOL supplies digital I/O pins TDO, TDI, TMS, TCK, TRSTn, RCLK1, RCLK2, LED, CONFIG, and CLK_SEL[1:0].
3. VDDOR supplies digital I/O pins PTP_TRIG_IN, RESETn, MDC, MDIO, and INTn.

Table 19: Do Not Connect

Pin #	Pin Name	Pin Type	Description
47	DNC0	No Connect	Do not connect. Do not connect this pin to anything.
55	DNC1		

Table 20: I/O State at Various Test or Reset Modes

Pin(s)	Loopback	Software Reset	Hardware Reset	Power Down
MDI[3:0]P/N	Active	Tri-state	Tri-state	Tri-state
U_OUTP/N	Active	Internally pulled up by terminations of 50 ohms	Internally pulled up by terminations of 50 ohms	Reg. 0_30.11 (Page 30, Register 0, bit 11) state 0 = Internally pulled up by terminations of 50 ohms 1 = Active
MDIO	Active	Active	Tri-state	Active
INTn	Active	Tri-state	Tri-state	Tri-state
TDO	Active	Active	Active	Active

1.2 Pin Assignment List

1.2.1 88E1780 128-Pin LQFP Package Pin Assignment List

Table 21: 88E1780 128-Pin LQFP List—Alphabetical by Signal Name

Pin Name	Pin Number
AVDD15	3
AVDD15	38
AVDD15	41
AVDD15	50
AVDD15	51
AVDD15	52
AVDD15	68
AVDD15	71
AVDD15	102
AVDD33	12
AVDD33	29
AVDD33	80
AVDD33	97
AVSS	44
AVSS	45
AVSS	49
AVSS	53
AVSS	57
AVSS	58
CLK_SEL[0]	107
CLK_SEL[1]	108
CONFIG[0]	118
CONFIG[1]	119
DNC0	47
DNC1	55

Pin Name	Pin Number
DVDD	59
DVDD	114
DVDD	116
HSDACN	39
HSDACP	40
INTn	61
MDC	63
MDIO	62
P0_LED[0]	110
P0_MDIN[0]	73
P0_MDIN[1]	75
P0_MDIN[2]	77
P0_MDIN[3]	79
P0_MDIP[0]	72
P0_MDIP[1]	74
P0_MDIP[2]	76
P0_MDIP[3]	78
P1_LED[0]	111
P1_MDIN[0]	87
P1_MDIN[1]	85
P1_MDIN[2]	83
P1_MDIN[3]	81
P1_MDIP[0]	88
P1_MDIP[1]	86
P1_MDIP[2]	84

Pin Name	Pin Number
P1_MDIP[3]	82
P2_LED[0]	112
P2_MDIN[0]	90
P2_MDIN[1]	92
P2_MDIN[2]	94
P2_MDIN[3]	96
P2_MDIP[0]	89
P2_MDIP[1]	91
P2_MDIP[2]	93
P2_MDIP[3]	95
P3_LED[0]	113
P3_MDIN[0]	105
P3_MDIN[1]	103
P3_MDIN[2]	100
P3_MDIN[3]	98
P3_MDIP[0]	106
P3_MDIP[1]	104
P3_MDIP[2]	101
P3_MDIP[3]	99
P4_LED[0]	121
P4_MDIN[0]	5
P4_MDIN[1]	7
P4_MDIN[2]	9
P4_MDIN[3]	11
P4_MDIP[0]	4
P4_MDIP[1]	6
P4_MDIP[2]	8
P4_MDIP[3]	10

Pin Name	Pin Number
P5_LED[0]	122
P5_MDIN[0]	19
P5_MDIN[1]	17
P5_MDIN[2]	15
P5_MDIN[3]	13
P5_MDIP[0]	20
P5_MDIP[1]	18
P5_MDIP[2]	16
P5_MDIP[3]	14
P6_LED[0]	124
P6_MDIN[0]	22
P6_MDIN[1]	24
P6_MDIN[2]	26
P6_MDIN[3]	28
P6_MDIP[0]	21
P6_MDIP[1]	23
P6_MDIP[2]	25
P6_MDIP[3]	27
P7_LED[0]	125
P7_MDIN[0]	36
P7_MDIN[1]	34
P7_MDIN[2]	32
P7_MDIN[3]	30
P7_MDIP[0]	37
P7_MDIP[1]	35
P7_MDIP[2]	33
P7_MDIP[3]	31
PTP_CLKN	66

Pin Name	Pin Number
PTP_CLKP	67
PTP_TRIG_IN	64
RCLK1	115
RCLK2	117
REF_CLKN	69
REF_CLKP	70
RESETn	60
RSET	42
TCK	128
TDI	1
TDO	127
TEST0	120

Pin Name	Pin Number
TMS	2
TRSTn	126
TSTPT	43
U_INN	48
U_INP	46
U_OUTN	54
U_OUTP	56
VDDOL	109
VDDOL	123
VDDOR	65
VSS	EPAD

2 Functional Details

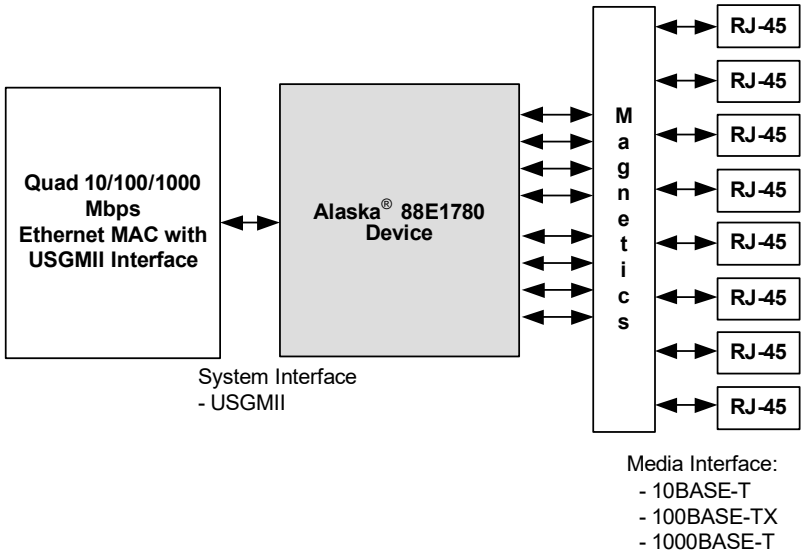
2.1 Modes of Operation and Major Interfaces

The device has two separate major electrical interfaces:

- MDI Interface to Copper Cable
- USGMII Interface

The MDI Interface is the media interface. The USGMII Interface is the system interface. (The system interface is also known as MAC interface. It is typically the connection between the PHY and the MAC or the system ASIC.) For example:

Figure 3: USGMII System to Copper Interface Example



2.2 LED

The device supports two modes of LED operation: one direct connect LED (LED[0]) per port OR two LEDs (LED[1:0]) per port in a 4x4 matrix configuration. The LEDs are programmable to indicate link, speed, and activity functions. The LEDs are by default configured to use Single LED Mode after hard-reset. To change the LED mode to Matrix LED Mode, write Reg 1_28.10 = `1'.

The Px_LED pins are used to drive LED pins. Registers 16_3, 17_3, 18_3, and 19_3 controls the operation of the LED pins. Px_LED pins are also used to configure the PHY per Section 2.3.1, Hardware Configuration, on page 24. After the configuration is completed, Px_LED pins will operate per this section.

Register 16_3.7:4 controls the LED[1] function and register 16_3.3:0 controls the LED[0] function. In a single LED mode, each of the Px_LED pin corresponds to the port's LED[0]. In matrix LED mode, the Px_LED are divided into rows and columns where the rows signal (RLED) connected to the anode of each LEDs and columns signal (CLED) connected to the cathode of each LEDs. Table 22 shows an example of implementation using matrix LED mode.

There are some LED modes where LED[1:0] operate as a unit. This is entered when register 16_3.3:2 is set to 11,which is referred to as dual LED modes. In dual LED modes, register 16_3.7:4 have no meaning when 16_3.3:2 is set to 11.

The LED reports the status of the copper media interface.

Figure 4 shows a Single LED mode example.

Figure 5 shows a Matrix LED mode example, and Table 22 shows LED mapping in Matrix LED mode.

Figure 4: Single LED Mode Example

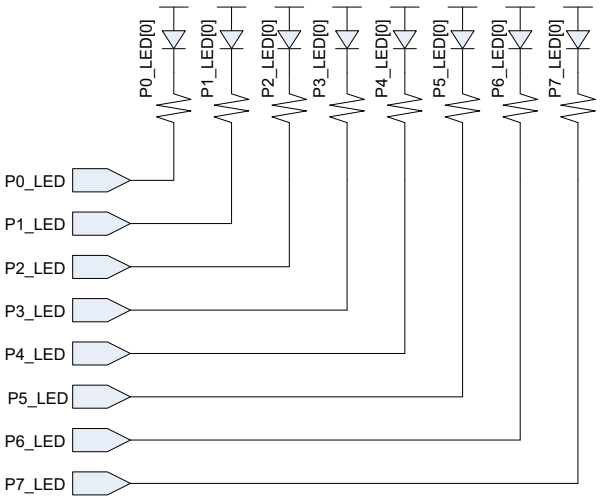


Table 22: LED Mapping

	CLED[0]/P0_LED	CLED[1]/P1_LED	CLED[2]/P2_LED	CLED[3]/P3_LED
RLED[0]/P4_LED	Port 0, LED[1]	Port 0, LED[0]	Port 1, LED[1]	Port 1, LED[0]
RLED[1]/P5_LED	Port 2, LED[1]	Port 2, LED[0]	Port 3, LED[1]	Port 3, LED[0]
RLED[2]/P6_LED	Port 4, LED[1]	Port 4, LED[0]	Port 5, LED[1]	Port 5, LED[0]
RLED[3]/P7_LED	Port 6, LED[1]	Port 6, LED[0]	Port 7, LED[1]	Port 7, LED[0]

Figure 5: Matrix LED Mode Example

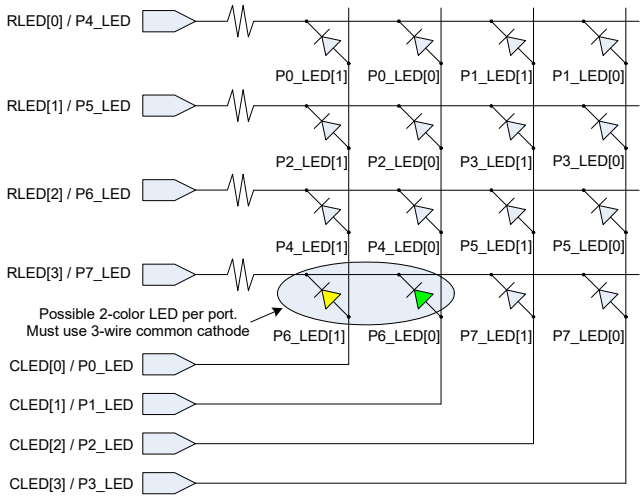
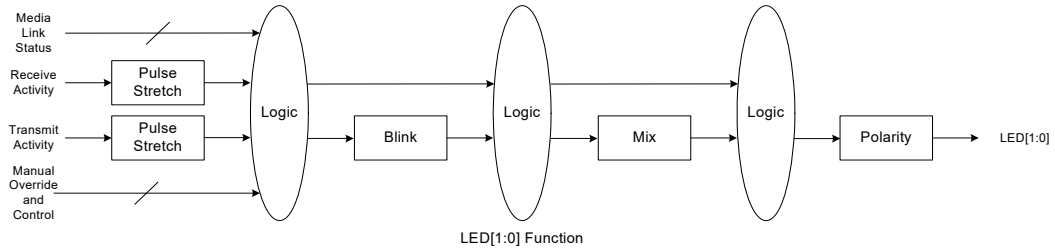


Figure 6 shows the general chaining of function for the LEDs. The various functions are described in the following sections.

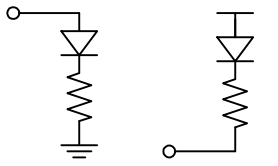
Figure 6: LED Chain



2.2.1 LED Polarity

There are two ways to hook up the LED in single LED mode as shown in Figure 4. In the matrix LED mode, the LEDs must be connected as shown in Figure 5. In order to make things more flexible registers 17_3.3:2, and 17_3.1:0 specify the output polarity for the LED[1:0] function. The lower bit of each pair specified the on (active) state of the LED, either high or low. The upper bit of each pair specifies whether the off state of the LED should be driven to the opposite level of the on state or Hi-Z. The Hi-Z state is useful in cases such the LOS and INIT function where the inactive state is Hi-Z.

Figure 7: Single LED Mode Configurations



Single LED - High Active | Single LED - Low Active

Table 23: LED Polarity

Register	LED Function	Definition
17_3.3:2	LED[1]	00 = On - drive LED[1] low, Off - drive LED[1] high 01 = On - drive LED[1] high, Off - drive LED[1] low 10 = On - drive LED[1] low, Off - tristate LED[1] 11 = On - drive LED[1] high, Off - tristate LED[1]
17_3.1:0	LED[0]	00 = On - drive LED[0] low, Off - drive LED[0] high 01 = On - drive LED[0] high, Off - drive LED[0] low 10 = On - drive LED[0] low, Off - tristate LED[0] 11 = On - drive LED[0] high, Off - tristate LED[0]

2.2.2 Pulse Stretching and Blinking

Register 18_3.14:12 specifies the pulse stretching duration of a particular activity. Only the transmit activity, receive activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

Some status will require blinking instead of a solid on. Register 18_3.10:8 specifies the blink rate. Note that the pulse stretching is applied first and the blinking will reflect the duration of the stretched pulse.

The stretched/blinked output will then be mixed if needed (Section 2.2.3) and then inverted/Hi-Z according to the polarity described in section (Section 2.2.1)

Table 24: Pulse Stretching and Blinking

Register	LED Function	Definition
18_3.14:12	Pulse stretch duration	000 = No pulse stretching 001 = 21 ms to 42 ms 010 = 42 ms to 84 ms 011 = 84 ms to 170 ms 100 = 170 ms to 340 ms 101 = 340 ms to 670 ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
18_3.10:8	Blink Rate	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved

2.2.3 Bi-Color LED Mixing

Bi-color LED mixing applies only when the LEDs are used in the matrix LED mode configuration. There is no mixing in the single LED mode. The bi-color LED mixing allows the two colors of the LED to be mixed to form a third color. This is useful since the PHY is tri speed and the three colors each represent one of the speeds. The LED color mixing can be done by controlling when the LED turned ON or OFF individually (by forcing the LED to be ON or OFF) or by enabling the dual LED mode. The dual LED mode mixing is enabled when register 16_3.3:0 are set to 11xx.

In dual LED mode, Register 17_3.15:12 control the amount to mix in the LED[1] pin. Register 17_3.11:8 control the amount to mix in the LED[0] pin. The mixing is determined by the percentage of time the LED is on during the active state. The percentage is selectable in 12.5% increments.

In this configuration, both of the LEDs can be turned on at the same time. Hence the sum of the percentage specified by 17_3.15:12 and 17_3.11:8 can exceed 100%.

Table 25: Bi-Color LED Mixing

Register	LED Function	Definition
17_3.15:12	LED[1] mix percentage	0000 = 0% 0001 = 12.5% . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
17_3.11:8	LED[0] mix percentage	0000 = 0% 0001 = 12.5%, . . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved

2.2.4 Modes of Operation

The LED pins relay some modes of the PHY so that these modes can be displayed by the LEDs.

Table 26: Modes of Operation

Register	LED Function	Definition
16_3.7:4	LED[1] Control	If 16_3.3:2 is set to 11 then 16_3.7:4 has no effect 0000 = On - Copper Link, Off - Else 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - 100 Mbps, Link or Fiber Link, Off - Else 0110 = On - 100/1000 Mbps Link, Off - Else 0111 = On - 100 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
16_3.3:0	LED[0] Control	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000 Mbps 2 blinks - 100 Mbps 1 blink - 10 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)

2.3 Configuring the Device

The device can be configured two ways:

- Hardware configuration strap options (unmanaged applications)
- MDC/MDIO register writes (managed applications)

The hardware configuration options (PHYADR[4:2] and PHY_ORDER) cannot be overwritten by software.

2.3.1 Hardware Configuration

After the deassertion of RESETn the device will be hardware configured.

The device is configured through the CONFIG pin and CLK_SEL[1:0]. By default, the device is configured in power down mode with a single LEDs per port after deassertion of RESETn. If Matrix LEDs are used, the Matrix LEDs can be enabled through software configuration.

CLK_SEL[1:0] are used to select the reference clock input option.

The CONFIG pin is used to configure 4 bits. The 4-bit value is set depending on what is connected to the CONFIG pin soon after the deassertion of hardware reset. The 4-bit mapping is shown in Table 27.

Table 27: Four Bit Mapping

Pin	Bit[3:0]
VDDOL	1111
P6_LED	1110
P5_LED	1101
P4_LED	1100
P3_LED	1011
P2_LED	1010
P1_LED	1001
VSS	0000

The 4 bits for the CONFIG pin is mapped as shown in Table 28.

Table 28: Configuration Mapping

Pin	Bit3	Bit 2	Bit1	Bit 0
CONFIG[0]	Reserved. Set to 0 or 1.	PHY_ORDER	PHYADR[4]	PHYADR[3]
CONFIG[1]	Reserved. Set to 0 or 1.	LED_MODE	PCH_EN	PWRDN

Each bit in the configuration is defined as shown in Table 29.

Table 29: Device Configuration Definition

Bits	Definition	Register Affected
PHYAD[4:3]	Two MSB of the 5-bit PHY address	None
PHY_ORDER	1 = PHYAD[2:0] is set as follows: Port 7 = 000 Port 6 = 001 Port 5 = 010 Port 4 = 011 Port 3 = 100 Port 2 = 101 Port 1 = 110 Port 0 = 111 0 = PHYAD[2:0] is set as follows: Port 0 = 000 Port 1 = 001 Port 2 = 010 Port 3 = 011 Port 4 = 100 Port 5 = 101 Port 6 = 110 Port 7 = 111	None
PDOWN	Power state of the PHY at power up: 1 = Power down 0 = Power up	0.11, 16_0.2
PCH_EN	0 = PCH is bypassed, 1 = PCH is not bypassed. PCH_EN will be the default value of PCH's TBD register bit, which will bypass the PCH logic. This TBD bit should be able to overwrite through MDIO interface.	28_14.10
LED_MODE	1 = Normal led mode 0 = Matrix led mode	28_1.10

2.3.2 Software Configuration - Management Interface

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3 Clause 22 and Clause 45 MDIO protocol. MDC is the management data clock input and, it can run from DC to a maximum rate of 12.5 MHz. At high MDIO fanouts the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC.

The MDIO pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm that pulls the MDIO high during the idle and turnaround.

PHY address is configured during the hardware reset sequence. Refer to Section 2.3.1, Hardware Configuration, on page 24 for more information on how to configure PHY addresses.

All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in the Register Description.

2.3.2.1 Clause 22 MDC/MDIO Management Interface

Typical read and write operations on the management interface are shown in Figure 8 and Figure 9.

Figure 8: Typical MDC/MDIO Read Operation

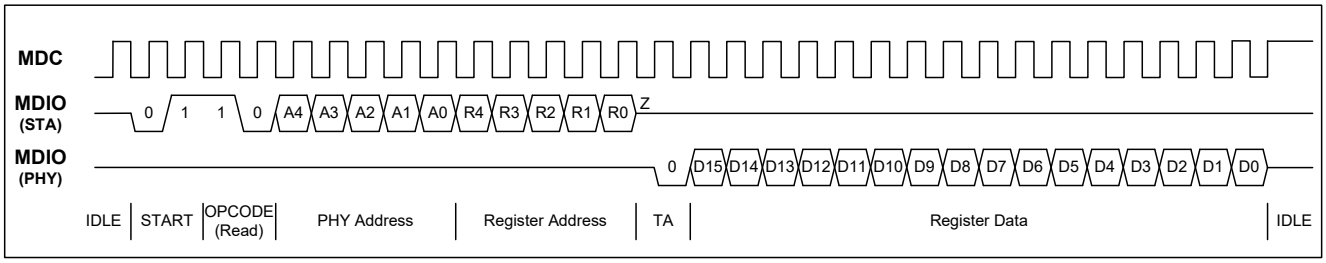


Figure 9: Typical MDC/MDIO Write Operation

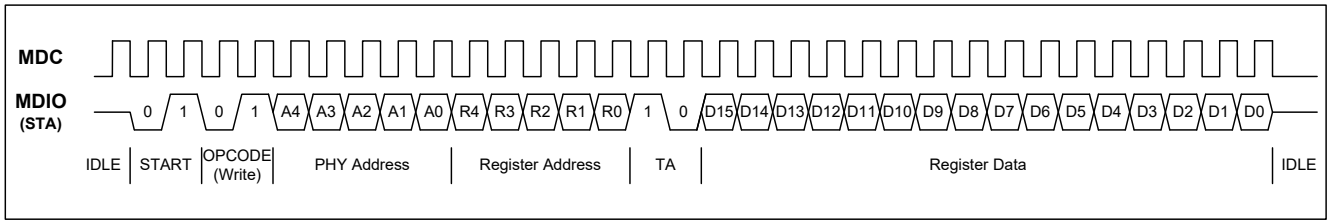


Table 30 is an example of a read operation.

Table 30: Serial Management Interface Protocol

32-Bit Preamble	Start of Frame	OpCode Read = 10 Write = 01	5-Bit PHY Device Address	5-Bit PHY Register Address (MSB)	2-Bit Turn around Read = z0 Write = 10	16-Bit Data Field	Idle
11111111	01	10	01100	00000	z0	0001001100000000	11111111

2.3.2.2 Extended Register Access

The IEEE defines only 32 registers address space for the PHY. In order to extend the number of registers address space available a paging mechanism is used. Register 22 bits 7 to 0 are used to specify the page. There is no paging for registers 22.

In this document, the short hand used to specify the registers take the form register_page.bit:bit, register_page.bit, register.bit:bit, or register.bit.

For example:

Register 16 page 2 bits 5 to 2 is specified as 16_2.5:2.

Register 16 page 2 bits 5 is specified as 16_2.5.

It takes four MDIO write commands to write the same register to the same value on all 8 ports. Register 22.15:14 can be used to selectively ignore PHYAD[4:2] and PHYAD[1:0] as shown in Table 31 so that the same register address can be written to all four ports in one MDIO write command. PHYAD[4:0] will still be decoded for read commands.

Care must be taken to setup multiple port write. To enable the concurrent write access write register 22 four times in a row with bit 14 set to 1 – once to each PHYAD[4:0]. The values written on all 16 bits must be the same otherwise unpredictable behavior will occur.

Once the four write commands to register 22 are issued, all subsequent writes will be concurrent to all ports including writes to register 22.

Concurrent write access will continue as long as every write to register 22 sets 22.14 to 1.

To disable concurrent write access simply write register 22.14 to 0.

Table 31: Page Address

Register	Function	Setting	Mode	HW Rst	SW Rst
22.15	Ignore PHYAD[4:2]	0 = Use PHYAD[4:2] to decode write commands 1 = Ignore PHYAD[4:2] to decode write commands	R/W	0	Retain
22.14	Ignore PHYAD[1:0]	0 = Use PHYAD[1:0] to decode write commands 1 = Ignore PHYAD[1:0] to decode write commands	R/W	0	Retain
22.13:8	Reserved	00000000	RO	0	0
22.7:0	Page select for registers 0 to 21, 23 to 31	Page Number	R/W	00	Retain

2.3.2.3 Clause 45 MDC/MDIO Management Interface (XMDIO)

Clause 45 provides extension of Clause 22 MDC/MDIO management interface to access more device registers while retaining its logical compatibility of the frame format. Clause 22 uses frame format with “Start of Frame” code of ‘01’ while Clause 45 uses frame format with “Start of Frame” code of ‘00’. The extensions for Clause 45 MDIO indirect register accesses are specified in Table 32.

Table 32: Extensions for Management Frame Format for Indirect Access

Frame	32-bit Preamble	Start of Frame	Opcode	5-bit PHY Address (MSB)	Device Address	2-bit Turnaround	16-bit ADRESS/DATA Field	Idle
Address	1..1	00	00	PPPPP	DDDDD	10	AAAAAAAAAAAAAAAA	Z
Write	1..1	00	01	PPPPP	DDDDD	10	DDDDDDDDDDDDDDDD	Z
Read	1..1	00	11	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z
Read Increment	1..1	00	10	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z

Clause 45 MDIO implements a 16-bit address register that stores the address of the register to be accessed. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, post-read increment-address cycles, the field contains the data for the register. At power up and reset, the contents of the register are undefined. Write, read, and post-read-increment-address frames access the address register, though write and read frames do not modify the contents of the address register.

2.3.2.4 Clause 22 Access to Clause 45 MDIO Manageable Device (MMD)

Clause 22 provides access to registers in a clause 45 MDIO MMD space using Register 13 and 14. Register 22.7:0 must be set to 0 to 7. If Register 22:7:0 is 8 to 255, the MMD registers are not accessible.

The MMD Access Control Register and Address/Data Register definitions are shown in Table 33 and Table 34.

Table 33: MMD Access Control Register
Page 0, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Function	R/W	0x0	0x0	15:14 00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only
13:5	Reserved	RO	0x000	0x000	Reserved
4:0	DEVAD	RO	0x00	0x00	Device address

Table 34: MMD Access Address/Data Register
Page 0, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Address Data	R/W	0x0000	0x0000	If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register.

Write Operation

To write to the MMD register access:

1. To Register 13, write the Function field to 00 (address) and DEVAD field with the device address value;
2. To Register 14, write the MMD's register address value;
3. To Register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value (as step #1);
4. To Register 14, write the content to be written to the selected MMD's register

Step 1 and 2 can be skipped if the MMD's address register was previously configured.

Read Operation

To read from the MMD register access:

1. To Register 13, write the Function field to 00 (address) and DEVAD field with the device address value;
2. To Register 14, write the MMD's register address value;
3. To Register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value (as step #1);
4. From Register 14, read the content from the selected MMD's register.

Step 1 and 2 can be skipped if the MMD's address register was previously configured.

Write/Read Operation with Post Increment Function

Function '10' can be used to increment the address after each read and write access. Function '11' can be used to increment the address after write operation only. Function '11' enables a read-modify-write capability for successive addressed registers within the MMD.

2.4 Power Supplies

The device requires three power supplies: 1.05V, 1.5V, and 3.3V. Additional power supplies may be required if 1.8V/2.5V is used for VDDOR/VDDOL.

Once the voltage is selected for the VDDO, the I/Os are not compatible with other voltage.

2.4.1 AVDD33

AVDD33 is used as 3.3V analog supply.

2.4.2 AVDD15

AVDD15 is the 1.5V supply. AVDD15 is used as the analog supply REF_CLKP, REF_CLKN, and PTP_CLKP/PTP_CLKN. AVDD15 is also used as USGMII SERDES, RESET, TSTPT and HSDACP/HSDACN supplies.

2.4.3 DVDD

DVDD is used for the digital logic. DVDD is the 1.15V digital supply.

2.4.4 VDDOL

VDDOL supplies the digital I/O pins for TDO, TDI, TMS, TCK, TRST, RCLK, LED, CONFIG, and CLK_SEL[1:0].

VDDOL requires 2.5V or 3.3V.

2.4.5 VDDOR

VDDOR supplies the digital I/O pins for PTP_TRIG_IN, RESET, MDC/MDIO, and INTn. VDDOR requires 1.8V, 2.5V, or 3.3V. The voltage selection is done at the deassertion of hardware reset. Once set, the I/O is not tolerant to other I/O voltage levels.

2.4.6 Power Supply Sequencing

On power-up, no special power supply sequencing is required.

3 Electrical Specifications

3.1 Absolute Maximum Ratings[1]

Table 35: Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
V_{DDA15}	Power Supply Voltage on AVDD15 with respect to VSS	-0.5		1.65	V
V_{DD}	Power Supply Voltage on DVDD with respect to VSS	-0.5		1.5	V
V_{DDA33}	Power Supply Voltage on AVDD33 with respect to VSS	-0.5		3.63	V
V_{DDOL}	Power Supply Voltage on VDDOL with respect to VSS	-0.5		VDDOL +10%	V
V_{DDOR}	Power Supply Voltage on VDDOR with respect to VSS	-0.5		VDDOR + 10%	V
V_{PIN}	Voltage applied to any digital input pin	-0.5		VDDO + 0.7V	V
$T_{STORAGE}$	Storage temperature	-55		+125[1]	°C

1. 125 °C is only used as bake temperature for not more than 24 hours. Long term storage (e.g weeks or longer) should be kept at 85 °C or lower.

1. On power-up, no special power supply sequencing is required.

3.2 Recommended Operating Conditions

Table 36: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDA15}[1]	AVDD15 supply	For AVDD = 1.5V	1.42	1.50	1.58	V
V_{DDA33}	AVDD33 supply	For AVDD33	3.13	3.3	3.47	V
V_{DD}[1]	DVDD supply	For DVDD at 1.15V	1.11	1.15	1.18	V
V_{DDOL}[1]	VDDOL supply	For VDDOL at 2.5V	2.38	2.5	2.63	V
		For VDDOL at 3.3V	3.13	3.3	3.47	V
V_{DDOR}[1]	VDDOR supply	For VDDOR at 1.8V	1.71	1.8	1.89	V
		For VDDOR at 2.5V	2.38	2.5	2.63	V
		For VDDOR at 3.3V	3.13	3.3	3.47	V
RSET	Internal bias reference	Resistor connected to V_{SS}		5000 ± 1% Tolerance		Ω
T_A	Commercial Ambient operating temperature		0		70[2]	°C
T_J	Maximum junction temperature				125[3]	°C

1. Maximum noise allowed on supplies is 50 mV peak-peak.
2. Commercial operating temperatures are typically below 70 °C, e.g, 45 °C ~55 °C. The 70 °C max is Marvell® specification limit
3. Refer to white paper on TJ Thermal Calculations for more information.

3.3 Package Thermal Information

3.3.1 Thermal Conditions for 128-pin, LQFP Package

Table 37: Thermal Conditions for 128-pin, LQFP Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient for the 128-Pin, LQFP package $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		22		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		16.5		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		15.5		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		15		°C/W
ψ_{JT}	Thermal characteristic parameter[a] - junction to top center of the 128-Pin, LQFP package $\psi_{JT} = (T_J - T_{top})/P$. P = Total power dissipation, T_{top}: Temperature on the top center of the package.	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.6		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.69		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		0.75		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		0.9		°C/W
θ_{JC}	Thermal resistance[a] - junction to case for the 128-Pin, LQFP package $\theta_{JC} = (T_J - T_C)/ P_{top}$ P_{top} = Power dissipation from the top of the package	JEDEC with no air flow		15.5		°C/W
θ_{JB}	Thermal resistance[a] - junction to board for the 128-Pin, LQFP package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		8		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

3.4 Current Consumption

3.4.1 Use current specifications for 88E1680

3.5 Digital I/O DC Operating Conditions

3.5.1 Digital Pins

Table 38: Digital Pins

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VIH	Input high voltage	All digital inputs	VDDO = 3.3V	2.0		VDDO + 0.6V	V
			VDDO = 2.5V	1.75		VDDO + 0.6V	V
			VDDO = 1.8V	1.26		VDDO + 0.6V	V
VIL	Input low voltage	All digital inputs	VDDO = 3.3V	-0.3		0.8	V
			VDDO = 2.5V	-0.3		0.75	V
			VDDO = 1.8V	-0.3		0.54	V
VOH	High level output voltage	All digital outputs	IOH = -4 mA	VDDO - 0.4V			V
VOL	Low level output voltage	All digital outputs	IOL = 4 mA			0.4	V
I_{ILK}	Input leakage current	With internal pull-up resistor				10 -50	uA
		All others without resistor				10	uA
CIN	Input capacitance	All pins				5	pF

3.5.2 LED Pins - Single LED Mode (Reg 1_28.10 = 0)

Table 39: LED Pins - Single LED Mode (Reg 1_28.10 = 0)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VOH	High level output voltage	All LED outputs	IOH = -10 mA	VDDO - 0.4V			V
VOL	Low level output voltage	All LED outputs	IOL = 10 mA			0.4	V
I_{MAX}	Total maximum current per LED	All LED pins				12.5	mA
I_{ILK}	Input leakage current	All LED pins				10 -50	uA
CIN	Input capacitance	All LED pins				5	pF

3.5.3 LED Pins - Matrix LED Mode (Reg 1_28.10 = 1)

Table 40: LED Pins - Matrix LED Mode (Reg 1_28.10 = 1)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VOH	High level output voltage	P[3:0]_LED/CLED	IOH = -100 mA	VDDO - 0.4V			V
VOL	Low level output voltage	P[7:4]_LED/RLED	IOL = 25 mA			0.4	V
I_{MAX}	Total maximum current per LED	P[3:0]_LED/CLED				100	mA
		P[7:4]_LED/RLED				25	
I_{MAX_LED}	Maximum current per LED[1]					25	
I_{ILK}	Input leakage current	All LED pins				10 -50	uA
CIN	Input capacitance	All LED pins				5	pF

1. The P[3:0]_LED/CLED 100 mA maximum current is applicable when driving four LEDs at the same time. The maximum current per LED is 25 mA.

3.6 Digital I/O AC Electrical Specifications

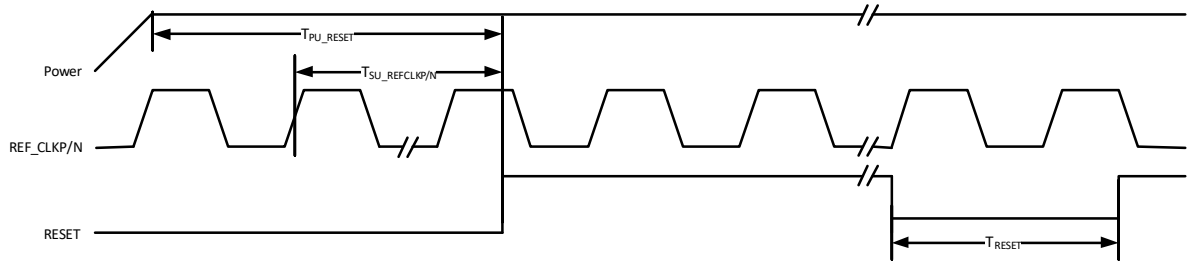
3.6.1 Reset Timing

Table 41: Reset Timing

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESET de-asserted		10			ms
$T_{SU\_REFCLKP/N}$	Number of valid REF_CLKP/N cycles prior to RESET de-asserted		10			clks
T_{RESET}	Minimum reset pulse width during normal operation		10			ms
T_{RESET_MDIO}	Minimum wait time from RESET de-assertion to first MDIO access		50			ms

Figure 10: Reset Timing



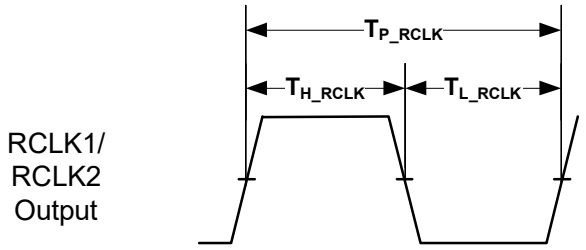
3.6.2 RCLK1/RCLK2 Output Timing

Table 42: RCLK1/RCLK2 Output Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_RCLK}	Period	125 MHz		8		ns
		25 MHz		40		ns
T_{H_RCLK}	High Time	125 MHz		4		ns
		25 MHz		20		ns
T_{L_RCLK}	Low Time	125 MHz		4		ns
		25 MHz		20		ns
T_{J_RCLK}	Total Jitter	125 MHz		750		ps
		25 MHz		555		ps

Figure 11: RCLK1/RCLK2 Output Timing

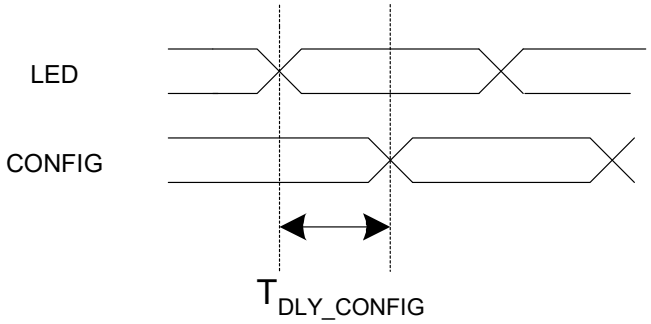


3.6.3 LED to CONFIG Timing

Table 43: LED to CONFIG Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_CONFIG}	LED to CONFIG Delay		0		25	ns

Figure 12: LED to CONFIG Timing



3.6.4 PTP Interface Timing

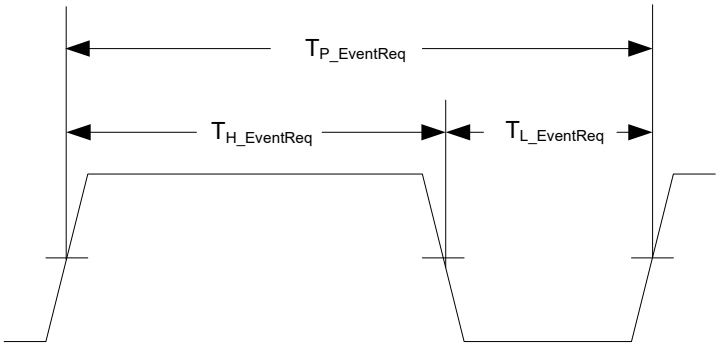
3.6.4.1 PTP Event Request Input AC Timing (PTP_TRIG_IN)

Table 44: PTP Event Request Input AC Timing (PTP_TRIG_IN)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_EventReq}$	Minimum gap between two PTP Event Request		150 ns + 5*PTP_-CLKP/NPer			ns, PTP_-CLKP/NPer
$T_{H\_EventReq}$	PTP Event Request Pulse Width		1.5 * PTP_-CLKP/NPer			PTP_-CLKP/NPer
$T_{L\_EventReq}$	PTP Event Request Low Time		1.5 * PTP_-CLKP/NPer			PTP_-CLKP/NPer

Figure 13: PTP Event Request Input Timing



3.6.5 MDC/MDIO Timing

Table 45: MDC/MDIO Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time		0		20	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time		10			ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time		10			ns
T_{P_MDC}	MDC Period		80			ns[1]
T_{H_MDC}	MDC High		30			ns
T_{L_MDC}	MDC Low		30			ns
V_{HYST}	VDDO Input Hysteresis			360		mV

1. Maximum frequency = 12.5 MHz.

Figure 14: MDC/MDIO Timing

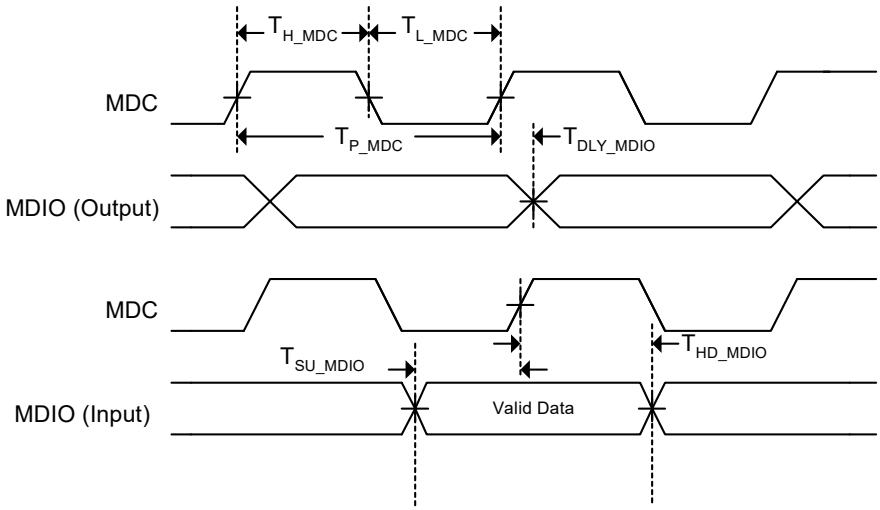
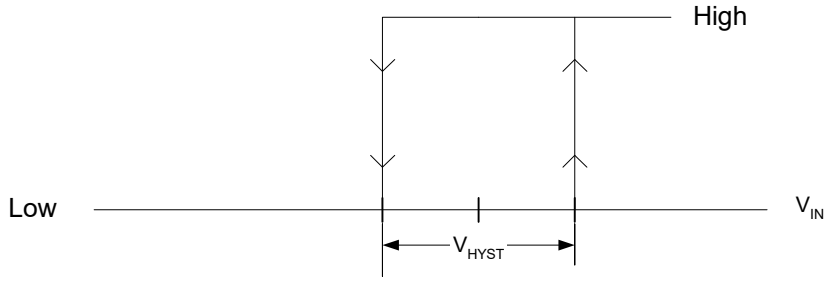


Figure 15: MDC/MDIO Input Hysteresis

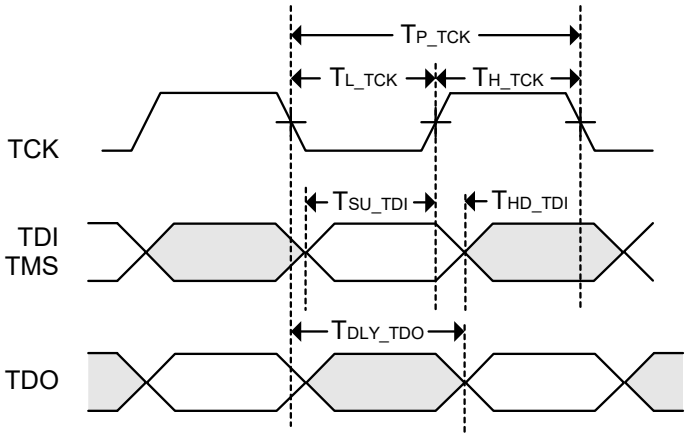


3.6.6 JTAG Timing

Table 46: JTAG Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period		60			ns
T_{H_TCK}	TCK High		12			ns
T_{L_TCK}	TCK Low		12			ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time		10			ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time		10			ns
T_{DLY_TDO}	TCK to TDO Delay		0		15	ns

Figure 16: JTAG Timing



3.7 Analog Electrical Specifications

3.7.1 IEEE DC Transceiver Parameters

Table 47: IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.
-10BASE-T IEEE 802.3 Clause 14
-100BASE-TX ANSI X3.263-1995

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute peak differential output voltage	MDIP/N[1:0]	10BASE-T no cable	2.2	2.5	2.8	V
		MDIP/N[1:0]	10BASE-T cable model	585[1]			mV
		MDIP/N[1:0]	100BASE-TX mode	0.950	1.0	1.050	V
		MDIP/N[3:0]	1000BASE-T[2]	0.67	0.75	0.82	V
	Overshoot[2]	MDIP/N[1:0]	100BASE-TX mode	0		5%	V
	Amplitude Symmetry (positive/ negative)	MDIP/N[1:0]	100BASE-TX mode	0.98x		1.02x	V+/V-
V_{IDIFF}	Peak Differential Input Voltage	MDIP/N[1:0]	10BASE-T mode	585[3]			mV
	Signal Detect Assertion	MDIP/N[1:0]	100BASE-TX mode	1000	460[4]		mV peak-peak
	Signal Detect De-assertion	MDIP/N[1:0]	100BASE-TX mode	200	360[5]		mV peak-peak

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. IEEE 802.3ab Figure 40 -19 points A&B.
3. The input test is actually a template test ; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The device will accept signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should de-assert signal detect (internal signal in 100BASE-TX mode). The Alaska V device will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

3.7.2 IEEE AC Transceiver Parameters

Table 48: IEEE AC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:
-10BASE-T IEEE 802.3 Clause 14-2000
-100BASE-TX ANSI X3.263-1995
-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall Time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
$T_{RISE/TFALL}$ Symmetry		MDIP/N[1:0]	100BASE-TX	0		0.5	ns
DCD	Duty Cycle Distortion	MDIP/N[1:0]	100BASE-TX	0		0.5[1]	ns, peak-peak
Transmit Jitter		MDIP/N[1:0]	100BASE-TX	0		1.4	ns, peak-peak

1. ANSI X3.263-1995 Figure 9-3

3.7.3 REFCLKP/N Receiver DC Specifications

Table 49: REFCLKP/N Receiver DC Specifications

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)
All voltages are given with respect to receiver circuit ground voltage

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_i	Input voltage range		0		AVDD15	V
V_{icm}	Input common mode voltage range		300		1300	mV
V_{icm_delta}	Variation of Input common mode				50	mV
$V_{id\ p\text{-}p}$	Input differential voltage peak-to-peak		200[1]		1200	mV
R_{in}	Receiver differential input impedance		80	100	120	Ω

1. For 125 MHz single-ended clock, the minimum amplitude is 400 mV. The unused pin must be connected with 0.1 μF capacitor to ground.

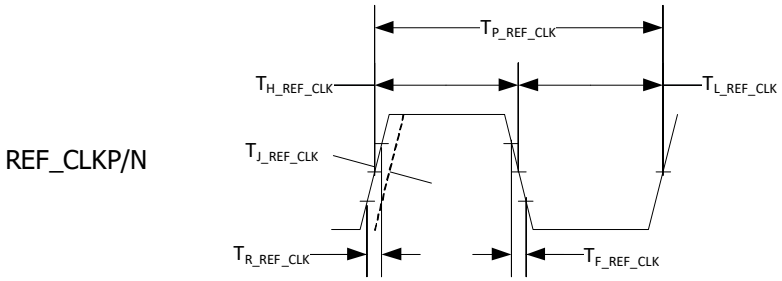
3.7.4 REFCLKP/N Receiver AC Specifications

Table 50: REFCLKP/N Receiver AC Specifications

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)
All voltages are given with respect to receiver circuit ground voltage

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_125\_REF\_CLK}$	125 MHz REF_CLK Period	CLK_SEL[1:0] = 01[1]	8 -50 ppm	8	8 +50 ppm	ns
$T_{H\_125\_REF\_CLK}$	125 MHz REF_CLK High Time		2.6	4	5.4	ns
$T_{L\_125\_REF\_CLK}$	125 MHz REF_CLK Low Time		2.6	4	5.4	ns
T_r/T_f	Rise and Fall Time (10% - 90%)		260	600	1280	ps
$T_{P\_156\_REF\_CLK}$	156.25 MHz REF_CLK Period	CLK_SEL[1:0] = 00[1]	6.4 -50 ppm	6.4	6.4 +50 ppm	ns
$T_{H\_156\_REF\_CLK}$	156.25 MHz REF_CLK High Time		2.1	3.2	4.3	ns
$T_{L\_156\_REF\_CLK}$	156.25 MHz REF_CLK Low Time		2.1	3.2	4.3	ns
T_r/T_f	Rise and Fall Time (10% - 90%)		260	480	1024	ps
t_{skew}	Skew tolerable at receiver input to meet setup and hold time requirements				325	ps
$T_{J\_REF\_CLK}$	REF_CLK Jitter (RMS)	12 kHz - 20 MHz (USGMII mode)			1	ps

Figure 17: REF_CLK Timing



3.7.5 PTP_CLKP/N Receiver DC Specifications

Table 51: PTP_CLKP/N Receiver DC Specifications

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)
All voltages are given with respect to receiver circuit ground voltage

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_i	Input voltage range		0		AVDD18	V
V_{icm}	Input common mode voltage range		300		1300	mV
V_{icm_delta}	Variation of Input common mode				50	mV
$V_{id\ p\text{-}p}$	Input differential voltage peak-to-peak		200		1200	mV
R_{in}	Receiver differential input impedance		80	100	120	Ω

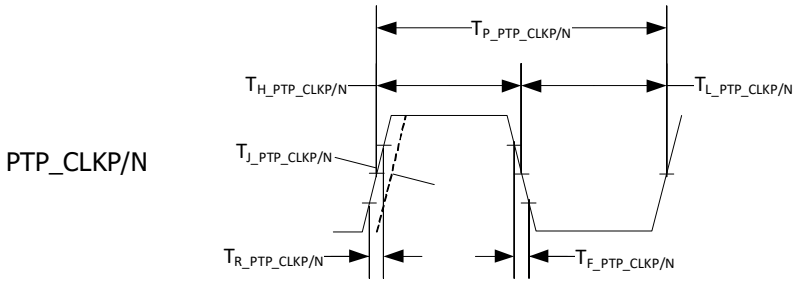
3.7.6 PTP_CLKP/N AC Specifications

Table 52: PTP_CLKP/N AC Specifications

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)
All voltages are given with respect to receiver circuit ground voltage

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_125\_PTP\_CLKP/N}$	125 MHz PTP_CLKP/N Period		8 -50 ppm	8	8 +50 ppm	ns
$T_{H\_125\_PTP\_CLKP/N}$	125 MHz PTP_CLKP/N High Time		2.6	4	5.4	ns
$T_{L\_125\_PTP\_CLKP/N}$	125 MHz PTP_CLKP/N Low Time		2.6	4	5.4	ns
T_r/T_f	Rise and Fall Time (10% - 90%)		260	600	1280	ps
t_{skew}	Skew tolerable at receiver input to meet setup and hold time requirements				325	ps
$T_{J\_PTP\_CLKP/N}$	PTP_CLKP/N Jitter (RMS)	12 kHz - 20 MHz (USGMII mode)			1	ps

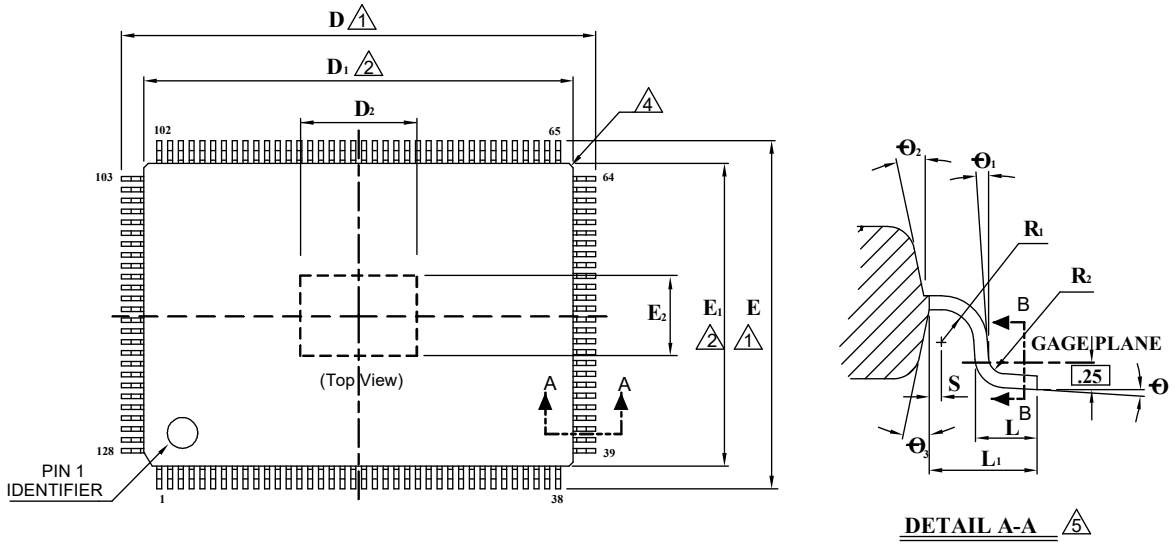
Figure 18: PTP_CLKP/N Timing

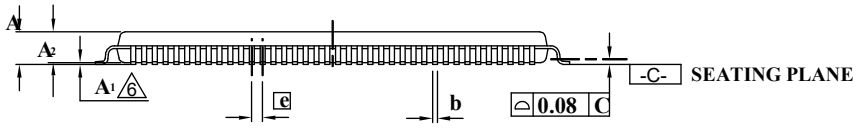


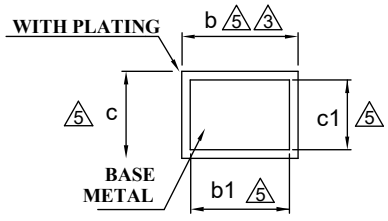
4 Mechanical Drawings

4.1 128-Pin LQFP Package Drawing

Figure 19: 128-Pin LQFP Package







NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
   D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS
   INCLUDING MOLD MISMACH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD
   BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE
   TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.

Table 53: 128-Pin LQFP Package Dimensions in mm

Symbol	Dimension in mm		
	Min	Nom	Max
A	--	--	1.60
A_1	0.05	--	0.15
A_2	1.35	1.40	1.45
b	0.17	0.22	0.27
b_1	0.17	0.20	0.23
c	0.09	--	0.20
c_1	0.09	--	0.16
D	21.90	22.00	22.10
D_1	19.90	20.00	20.10
E	15.90	16.00	16.10
E_1	13.90	14.00	14.10
e	0.50 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08	--	--
R_2	0.08	--	0.20
S	0.20	--	--
θ	0°	3.5°	7°
θ_1	4° TYP		
θ_2	12° TYP		
θ_3	12° TYP		
Exposed Pad Size			
D_2	5.41		
E_2	4.29		

5 Order Information

5.1 Ordering Part Numbers and Package Markings

Figure 20 shows the ordering part numbering scheme for the device. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 20: Sample Part Number

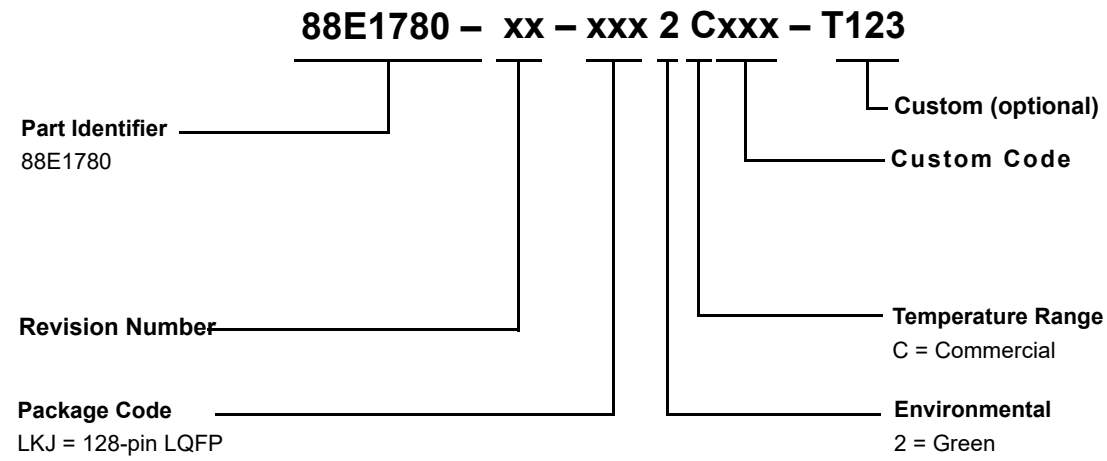


Table 54: Part Order Numbers

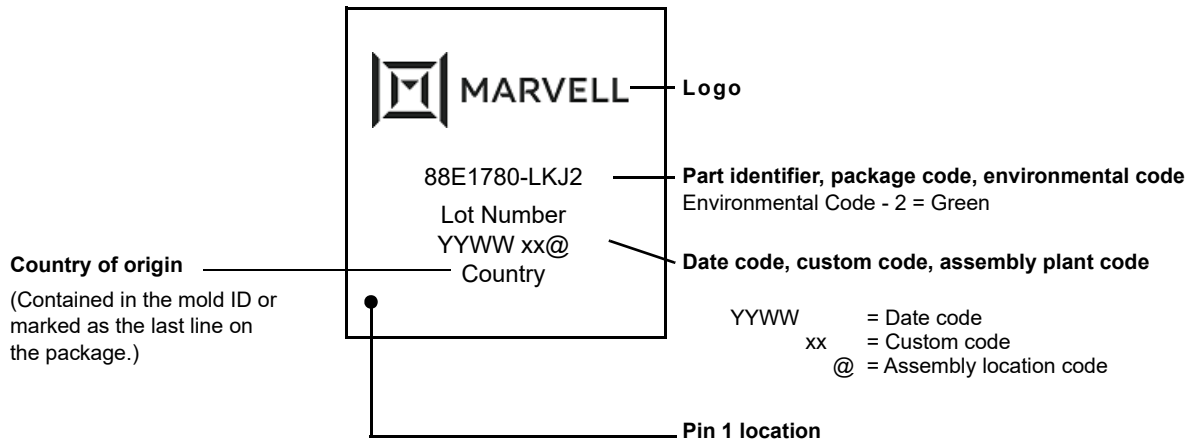
Package Type	Part Order Number
88E1780 128-pin LQFP - Commercial	88E1780-xx-LKJ2C000

5.1.1 Package Marking Examples

Figure 21 is an example of the package marking and pin 1 location for the 88E1780 128-pin LQFP commercial Green package.

.

Figure 21: 88E1780 128-pin LQFP Commercial Green Package Marking and Pin 1 Location for device



Note: The above example is not drawn to scale. Location of markings is approximate.

Marvell first revolutionized the digital storage industry by moving information at speeds never thought possible. Today, that same breakthrough innovation remains at the heart of the company's storage, networking and connectivity solutions. With leading intellectual property and deep system-level knowledge, Marvell semiconductor solutions continue to transform the enterprise, cloud, automotive, industrial, and consumer markets. For more information, visit www.marvell.com.

Doc. No. TD-000923 Rev. 1 Revised: October 5, 2020